Challenges of long term process stability and solutions for better control

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ABSTRACT

Maintaining the stability of all litho process parameters over time is crucial to ensuring consistent litho process yield throughout the product lifetime. The sensitivity of litho process performance to variations in litho process parameters is getting higher as processes use lower k1 and resist dimensions get smaller. The dependence of litho cell yield on a laser parameter change was investigated through simulations of memory patterns for various k1 and process layers by varying bandwidth control level of laser. The sensitivity of litho yield to laser bandwidth became higher when lower k1 imaging was used. Different bandwidth control requirements were determined based on the difference in CD control requirement of each layer as well as the difference in process window of the layout. Overall, tighter bandwidth control was required as pattern size and k1 became smaller. Significant improvements in long term process stability were achieved after implementation of low bandwidth variation operation at a production fab. Cymer's latest bandwidth control technology fulfills bandwidth control requirement for the simulated 43nm DRAM case, which has 0.31 k1 with 1.35NA ArF immersion lithography

Keywords: Long term stability, bandwidth control, litho yield, process stability, low k1 imaging

1. INTRODUCTION

The number of litho process steps has been increasing as technology progresses. In memory litho processing, more low k1 imaging layers, which have limited process window for selective patterns and high sensitivity to process variation, have been used as process integration gets more complicated. Maintaining high yield of the litho process is crucial to ensure product yield after multiple low k1 litho processes. Understanding the correlation between litho yield and each litho process parameter is important in setting the right control target for each process parameter. Litho process impacts, such as OPC curve change and pattern shape change, due to bandwidth have been reported in multiple studies [1]-[6] and accurate simulation methods have been established [7]. In this paper, we examined the litho yield impact due to bandwidth variation and determined the bandwidth control targets for future memory products as well as current products through simulations. We confirmed the benefit of tighter bandwidth control by evaluating real production fab data.

1.1 CD error sources of the Litho cell

CD error sources in the litho cell can come from various processes. Many process parameters, outside the litho cell as well as within the litho cell, influence litho process yield. It would be very complicated and lengthy to describe all the process parameter controls embedded in litho process tools enabling stable litho process performance. Here we describe some well known major CD error contributors. Poor film deposition uniformity of under layers such as BARC, bottom anti reflective coating, and resist can cause intra wafer CD change. In the track systems, not only changes in the resist coating and development process but also PEB temperature changes, delay changes between process modules and ambient contamination level changes can change resist CDs on the wafer. The exposure system has most sources of potential CD errors. Any change in the source, such as size, position and polarization, can create CD errors. Changes in the pupil characteristics of the projection lens, such as aberration, transmission, flare, and birefringence can also be sources of CD errors. Drift of best focal position and dose control also cause CD errors. Changes in light source characteristics may also cause CD error by changing the exposure tool parameters.

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1.2 CD errors by light source parameters

Since the laser supplies the light to exposure system, any CD change due to changes in laser parameters comes through changes in the corresponding exposure system imaging parameter. Table 1 explains the relationship and how the laser monitors and controls these parameters. It is challenging to set the correct control target for the laser parameters because CD error depends on the sensitivity of the exposure system to variations which can be different for different integrated exposure system. Therefore it is important to build accurate correlation between laser parameters and wafer performance for various exposure conditions in collaboration with the exposure system manufacturers. Currently, the bandwidth of laser can be modeled with high accuracy through simulations if chromatic aberrations of the projection lens are known. Wafer image impact due to other laser parameters are very dependent on each exposure systems' illuminator and projection optics design, so here we will only discuss wafer CD impact due to bandwidth changes. Therefore, all laser parameters are monitored and controlled to hard limits, which were agreed with the exposure system manufacturers to meet imaging requirements.

Laser parameters	Scanner Parameters	Monitoring and Control
Wavelength	**Focal position, Aberrations**	**WL Error, WL sigma, WL calibration**
Bandwidth	**Contrast Degradation**	**E95, FWHM**
Energy	**Dose control**	**Dose Error**
Beam parameters (pointing, divergence, shape)	**Illumination Source size And shape**	**Field metrology**

Table 1. Relationship between exposure tool's parameter to laser parameter, and the monitoring and control method for the laser parameters

2. SIMULATIONS AND FAB DATA ANALYSES

As we see from Figure 1, memory cell patterns are very repetitive and dense, so it is possible to optimize RET (Resolution Enhancement Technique) to maximize the printability of the cells. The RET provides large process window for dense cell patterns, but requires layout optimizations, such as dummy patterns, scattering bars, tighter process controls, or allowing larger CD tolerance for non-dense patterns.

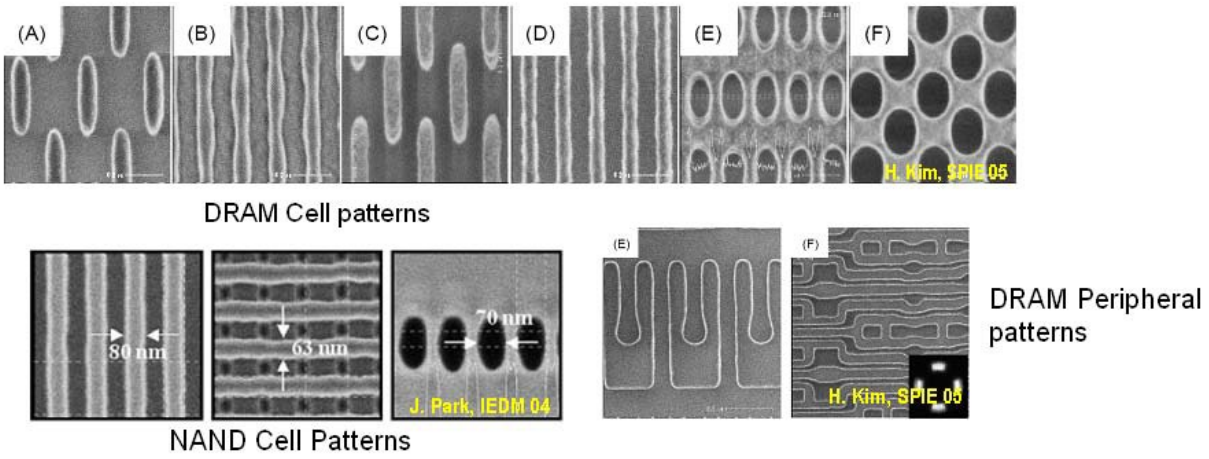
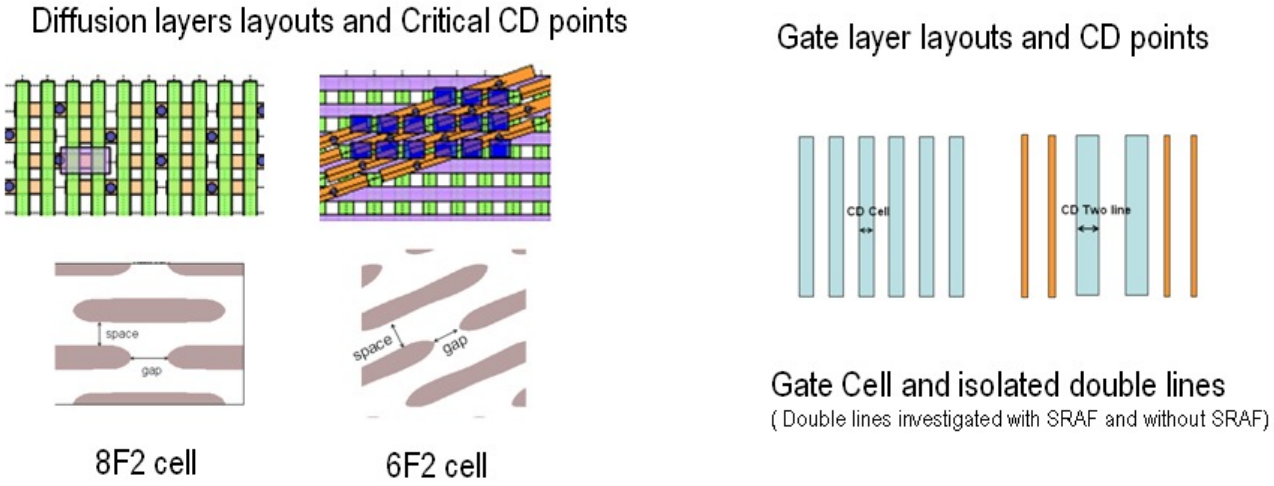


Figure 1. Typical memory patterns [8],[9]

Allowable wafer CD variations can be different for different layers, such as gate layer versus wire layer, and the sensitivity of CD variation to bandwidth can be different depending on layout and k1 factor. Two DRAM layers were simulated to understand the allowable bandwidth variations in order to maintain high litho yield. Two types of isolation layout styles, 6F cell and 8F cell, and two types of RET for two-line gate patterns, with SRAF and without SRAF, were investigated. Two NA, 0.93 and 1.35, and two k1 values, 0.34 and 0.31, were used. 71nm, 62nm, 49nm and 43nm half pitch were set as the target for the dense cell and 1.5X the target CD was used for isolation gap and two-line gate. SRAFs (Sub Resolution Assist Feature) were optimized for each simulation. A total of 20 cases were investigated. (Figure 2.)



Layout	Cell style	Illumination type	Pattern size
DRAM diffusion	2 (8F2, 6F2)	Annular	4 (half pitch:71nm, 62nm, 49nm, 43nm) (k1 0.34 & k1 0.31 for 0.93NA & 1.35NA)
DRAM gate	3 (cell, two line with SRAF)	Annular	4 (same as above)

Figure 2. Layouts and exposure conditions used for sensitivity study of litho yield to bandwidth change

2.1 Analysis method

Without any bandwidth error, litho yield was assumed to be 99.73%, which is a well centered Gaussian distribution. When bandwidth was changed, a CD shift was applied as predicted by simulations of each pattern. The new litho yield was calculated after applying a center shift of all CD values to the spec values.(Figure 3.) CD specifications were set differently by layer; +/- 3% of target CD for the gate layer and +/- 8% for the gap of the isolation layer.

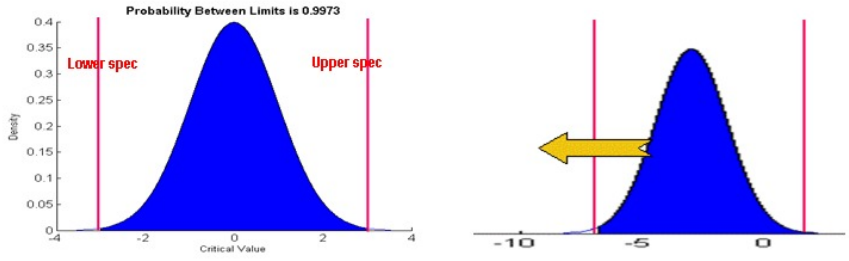


Figure 3. Litho yield calculation after CD shift due to bandwidth change

2.2 Isolation layers

For the end gap of the 8F cell, the CD sensitivity to bandwidth change increased at lower k1, from 0.5nm/0.1pm to 1.2nm/0.1pm, and the bandwidth control requirement became tighter at lower k1. For 0.34 k1, there was negligible litho yield change for +/-100fm E95 variation. For 0.31k1, +/- 50fm control of E95 would maintain litho yield. (Figure 4.)

For the end gap of the 6F cell, the CD sensitivities to bandwidth change were generally higher than the 8F case, 0.9nm/0.1pm for 0.34 k1 and 1.6nm/0.1pm for 0.31k1. Bandwidth control of +/- 100fm is good enough for 0.34k1, but +/-30fm level control would be desired for the 0.31k1 case. (Figure 5.)

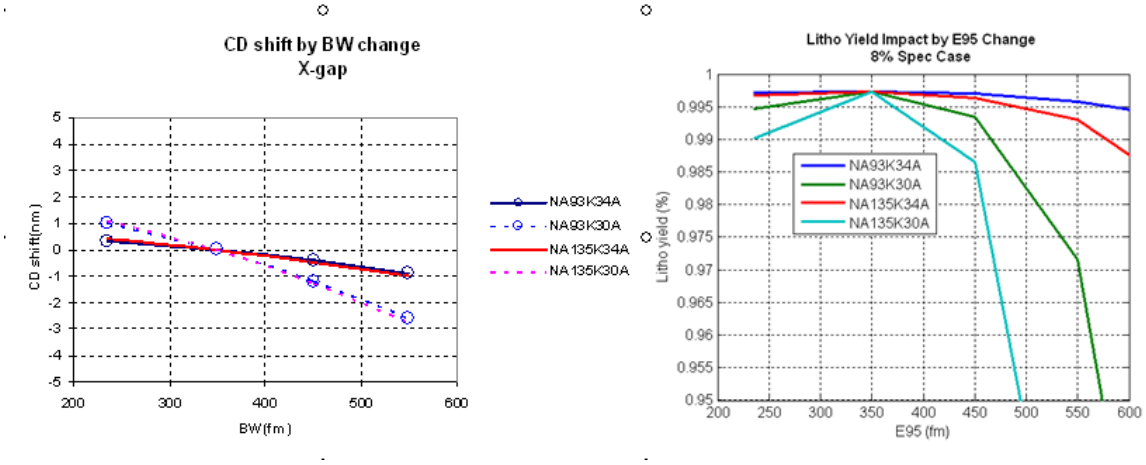


Figure 4. CD vs. BW and litho yield change due to BW for 8F cell isolation patterns.

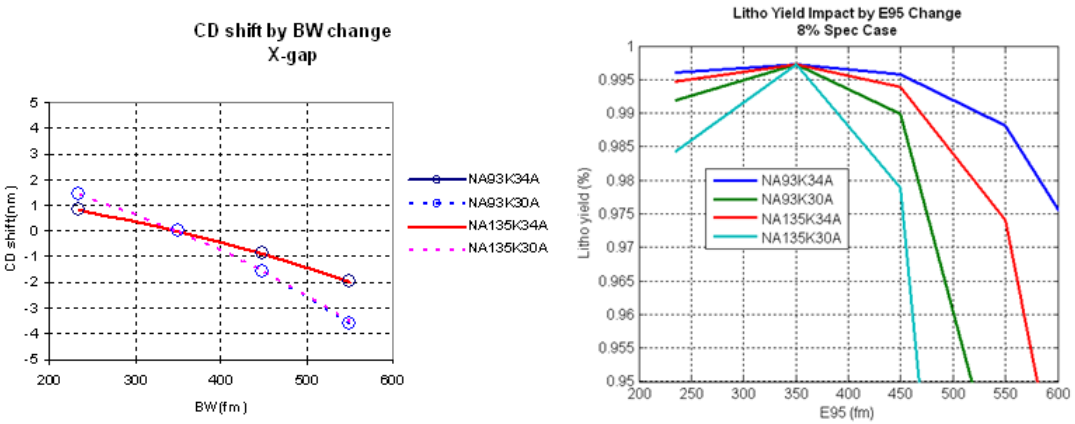


Figure 5. CD vs. BW and litho yield change due to BW for 6F cell isolation patterns.

2.3 Gate layers

For the cell of the gate layer, CD sensitivity to bandwidth change is minimal, <0.3nm/0.1pm, since the patterns are simple dense lines and spaces patterns. All cases showed negligible litho yield change for +/-100fm E95 change. For the 43nm case, +/-50fm E95 control would minimize any potential litho yield change. (Figure 6.) Two-line gate patterns show minimal dependence on k1 for most cases. SRAF reduced the CD sensitivity to bandwidth change by about 30%, from 1nm/0.1pm to 0.7nm/0.1pm. (Figure 7 ,8) Two-line gate patterns with SRAF require +/-30fm E95 control for 49nm and 43nm cases and two-line gate patterns without SRAF require +/-15fm E95 control, which can be challenging to achieve, to keep litho yield high above 99% level.

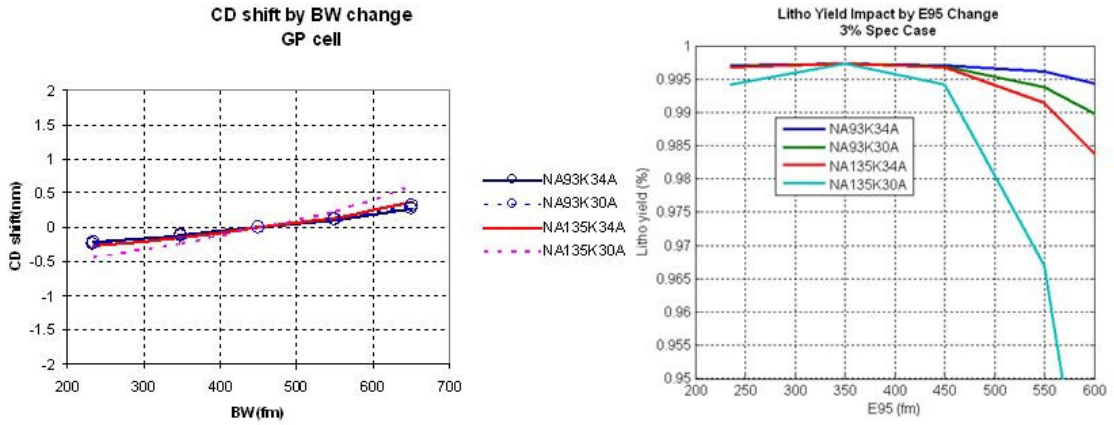


Figure 6. CD vs. BW and litho yield change due to BW for cell of gate layer

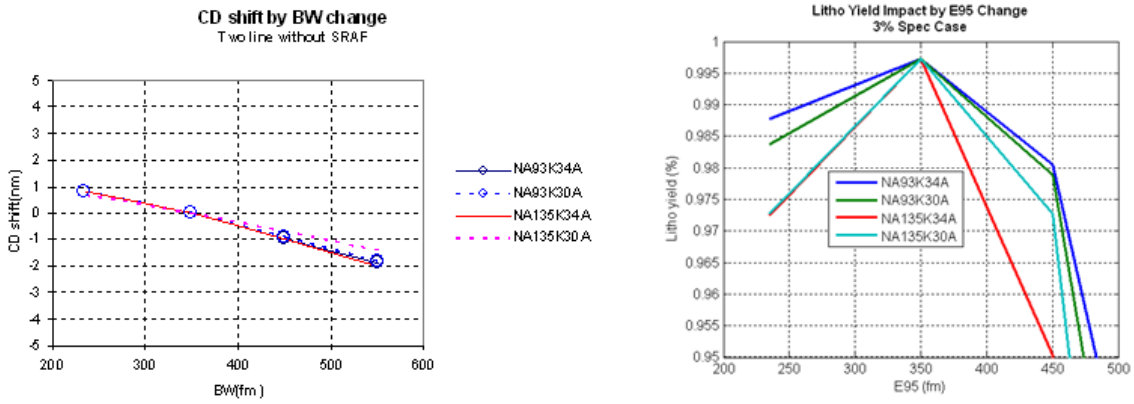


Figure 7. CD vs. BW and litho yield change due to BW for two-line gate without SRAF

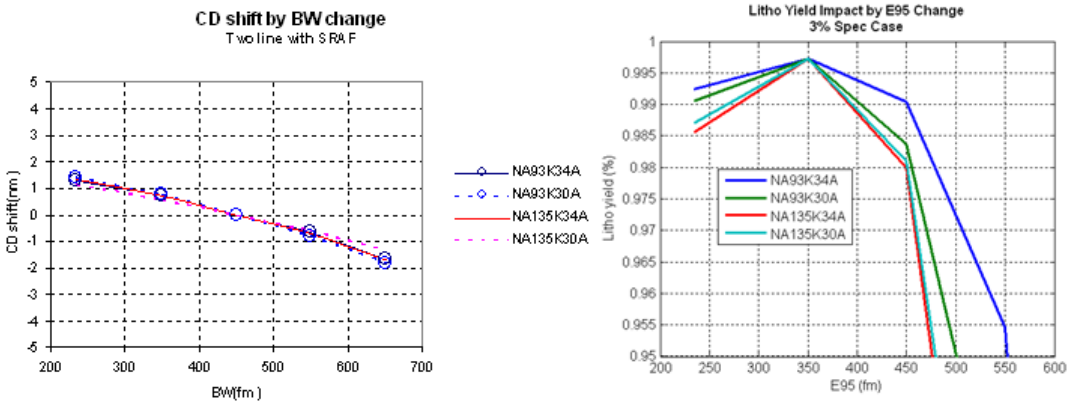
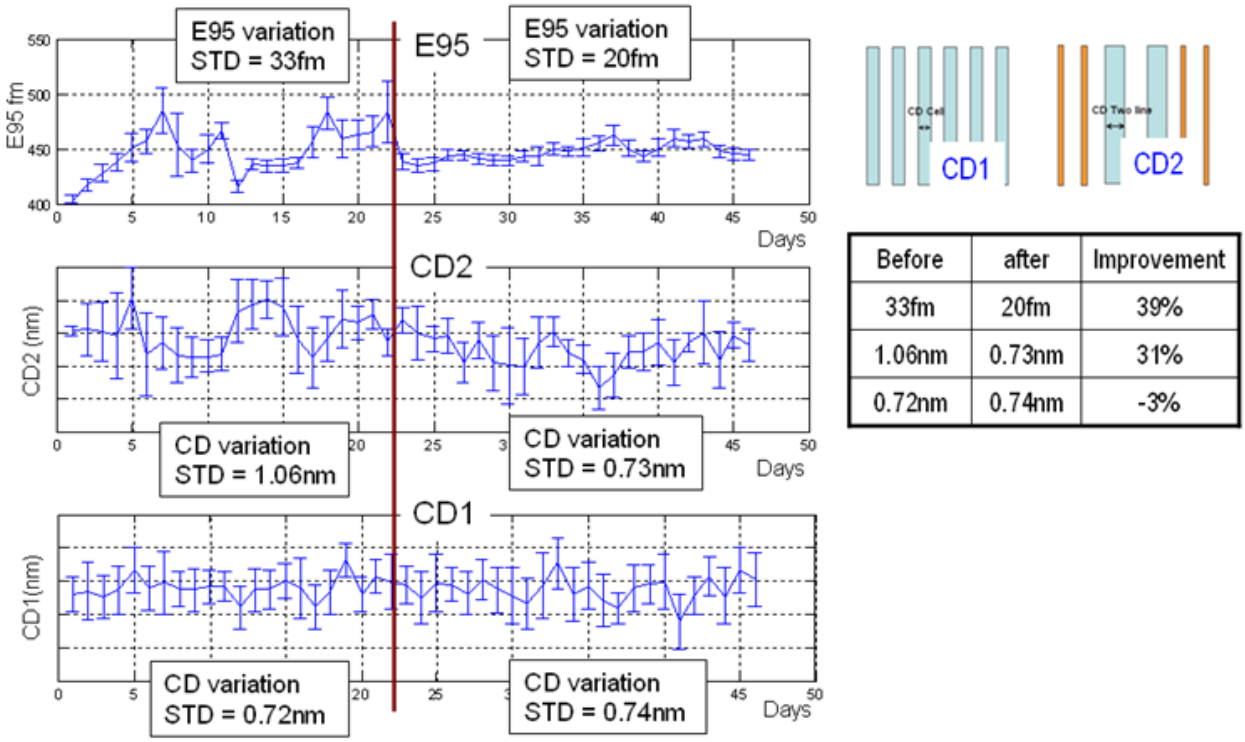


Figure 8. CD vs. BW and litho yield change due to BW for two-line gate with SRAF.

2.4 Fab data

Thousands of CDs and laser bandwidth values were monitored for two months at a real production fab line. Laser bandwidth control was improved around the middle of the monitoring period by implementing new laser modules for improved bandwidth control. As Figure 9 shows, the CDU of CD2, which is a two-line gate pattern with SRAF, matched well with the simulation study case, and improved by 31% due to bandwidth control improvement of 39% while CDU of CD1 showed no impact on bandwidth control improvement.



Before	after	Improvement
33fm	20fm	39%
1.06nm	0.73nm	31%
0.72nm	0.74nm	-3%

Figure 9. Correlation of CDU of CD1 and CD2 to BW data from production fab

3. DISCUSSION AND SUMMARY

Through simulations of DRAM patterns, we determined the dependence of E95 control requirements on the pattern layout and CD control target of the patterns. 6F isolation cell patterns require tighter bandwidth control than 8F cell patterns and two-line gate patterns require the tightest E95 control among the simulated cases. Overall, the 43nm generation requires tighter E95 control, 30 fm for the two-line gate and 50fm for other layouts. Fab data confirmed that the CDU of the two-line gate can be improved significantly by tighter bandwidth control.

Cymer has improved bandwidth control technology about 10X since the firstArF lasers by introducing both passive and active control technologies. (Figure 10.) Long term E95 stability of 23fm, reported from field data of a XLR-500i, which is a laser designed for use with immersion scanners, already exceeds the 43nm bandwidth control requirement from the simulated cases (Figure 11). Cymer bandwidth stabilization technologies are aligned to new lithography process requirements as lithography technology migrates to more advanced designs. Cymer's latest bandwidth control technology in the XLR-600i will improve bandwidth control by about 50% compared to the XLR 500i (Figure 12.) This will provide the bandwidth control performance needed for future litho processes beyond 43nm.

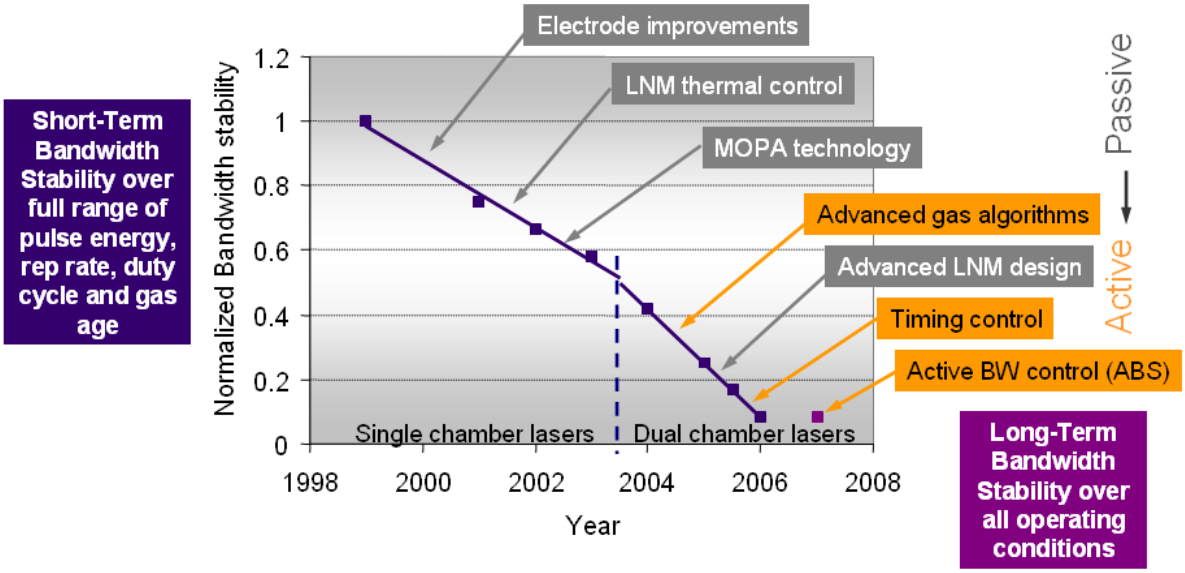


Figure 10. Cymer technology to support bandwidth control requirements.

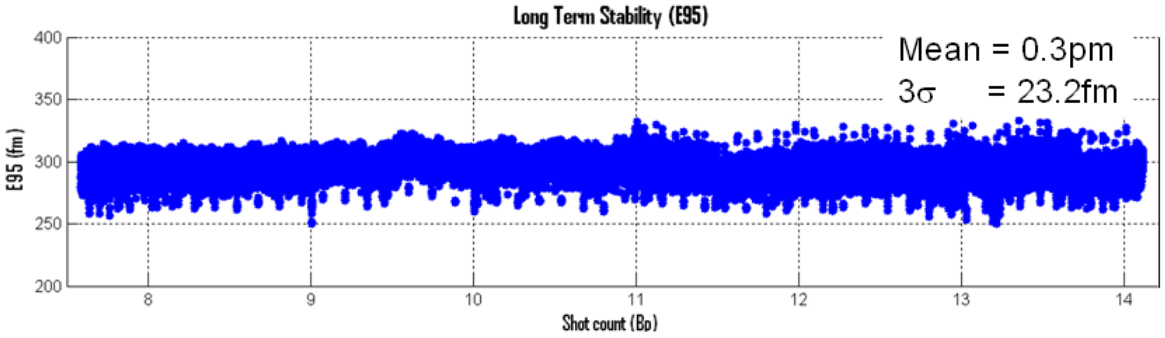


Figure 11. A field data of long term E95 stability from XLR 500i

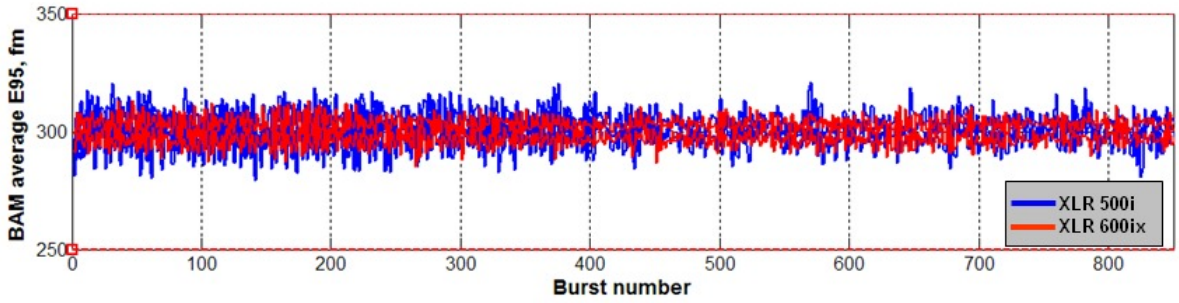


Figure 12. The latest BW control technology of XLR-600ix achieves 50% improvement compared to the XLR-500i.

REFERENCES

[1] I. Lalovic et al., "Effects of illumination spectral width on mask error enhancement factor and iso-dense bias in 0.6NA KrF imaging," Proc. SPIE Phot. Tech. Symp. BACUS XXI 4562 (2001).

[2] Brunner et al, "Laser bandwidth and other sources of focus blur in lithography," Proc. SPIE Optical Microlithography XIX 6154 (2006).

[3] Yoshimochi et al, "Study of iso-dense bias (IDB) sensitivity to laser spectral shape at the 45-nm node," Proc. SPIE Optical Microlithography XX 6520 (2007).

[4] K. Huggins et al., "Effects of laser bandwidth on OPE in a modern lithography tool," Proc. SPIE Optical Microlithography XIX 6154 (2006).

[5] Peter De Bisschop et al., "Impact of finite laser bandwidth on the critical dimension of L/S structures," J. Micro/Nanolith. MEMS MOEMS, Vol. 7, 033001 (2008)

[6] N. Seong et al., "Analyses of the effect of laser bandwidth on imaging of memory patterns," Proc. SPIE, Vol. 7140 (2008)

[7] I. Lalovic et al., "Fast and accurate laser bandwidth modeling of optical proximity effects",Proc. SPIE, Vol. 6730, 67301X (2007)

[8] H. Kim et al., "Implementation of KrF 0.29 k1 Lithography", Proc of SPIE Vol. 5754, (2005)

[9] J. Park et al., "8Gb MLC NAND Flash Memory using 63nm Process Technology", IEDM (2004)